By way of a second example, FIG. 5 can be modified to include, immediately after AND gates A163–A178, a plurality of up to sixteen, 1-to-2-of-N steering switches (see 431) that are programmable to steer the respective PT signal either to the OE terminal of the respective tristate driver 526 or to at least one, other wise programmably-specified control terminal, for example, selected ones of the OE controls of tristate longline drivers 586. If the PT output signal of such modified AND gates A163–A178 is steered away from the respective OE terminal, then the 1-to-2-of-N steering switch is further programmable to apply one or the other of an output enabling level (OE=1) or output disabling level (OE=0) to its respective tristate driver 526. Of course, by inserting such steering switches between AND gates A163–A178 and the OE terminals, the propagation time for OE-controlling PT's is increased and the size of the CPLD configuration memory is increased. Thus the design shown in FIG. 5 is faster and simpler.

By way of a third example, the OSM 570 in FIG. 5 can be modified to have more than 32 H-lines, where the additional H-lines (up to 32 more) are represented as 523 and receive respective MFB signals from one or more other SLB's. This allows SLB 510 to 'lend' or 'donate' its pads (516) for the outputting of result signals from the other SLB's if SLB 510 is not itself using such pads (516, buried or not) for the outputting of result signals. Of course, by inserting such additional pad sharing functionality, signal delays through the modified OSM and along lengthened MFB buses (522) may increase disadvantageously. Also, the size of the CPLD configuration memory will be increased to support the additional flexibility and the size of the IC die will increase commensurately. Thus the design shown in FIG. 5 is faster, smaller, simpler and cheaper to manufacture.

Given the above disclosure of general concepts and specific embodiments, the scope of protection sought is to be defined by the claims appended hereto.

What is claimed is:

1. A global switch matrix (GSM) for use within a programmably configurable integrated circuit (IC), where the IC has a first plurality, S of segments distributed within a logic-functions providing region of the IC, where each segment has one or more logic blocks, said global switch matrix providing programmably-definable interconnection between logic blocks of different ones of said segments and said GSM comprising:

(a) a second plurality, L of longlines extending across the logic-functions providing region of the IC;

(b) a third plurality, F of GSM-feeding lines crossing with the longlines and extending into the logic-functions providing region for coupling GSM-feed signals to the GSM, the GSM-feed signals including logic result signals produced by logic blocks of the S segments;

(c) a fourth plurality, M of programmably-controllable multiplexers each having an output port and a fifth plurality, N of input receiving points, each input receiving point being operatively coupled to a respective one of the F GSM-feeding lines,

(c.1) wherein the output port of each of the programmably-controllable multiplexers can be programmably switched between a high impedance state and an active state; and

(c.2) wherein respective subsets of M/L of the M multiplexers are distributively disposed along and coupled to respective ones of the L longlines.

2. The global switch matrix of claim 1 wherein:

(a.1) the second plurality, L is sufficiently large so that the L longlines can provide full intercoupling of logic result signals output from a first segment for input to a second segment and so that the L longlines can simultaneously provide full intercoupling of logic result signals output from the second segment for input to the first segment.

3. The global switch matrix of claim 2 wherein:

(a.1a) each segment can output a sixth plurality, R of logic result signals and the second plurality, L is greater than two times R.

4. The global switch matrix of claim 3 wherein:

(b.1) the GSM-feed signals further include input signals that are acquirable from outside the IC; and

(a.1b) L is sufficiently large to carry not only two times R of said logic result signals but to also additionally carry a plurality of said input signals.

5. The global switch matrix of claim 4 wherein L is at least 384.

6. The global switch matrix of claim 1 wherein:

(c.3) respective ones of the F GSM-feeding lines each couple to a plural number of said input receiving points, where the plural number of input receiving points are distributed amongst plural ones of the programmably-controllable multiplexers so that a given GSM-feed signal, on a respective one of the GSM-feeding lines, has more than one way of feeding into a longline of the GSM.

7. The global switch matrix of claim 1 wherein:

(b.1) respective subsets of said F GSM-feeding lines that couple GSM-feed signals from respective but different ones of the segments are intertwined as the respective subsets of GSM-feeding lines cross with the longlines.

8. The global switch matrix of claim 1 wherein the GSM further comprises:

(d) a sixth plurality, G of segment-feeding lines crossing with the longlines and extending into the logic-functions providing region for coupling GSM-sourced signals from the GSM to corresponding ones of the segments,

(d.1) wherein respective subsets of said G segment-feeding lines that couple GSM-sourced signals to respective but different ones of the segments are intertwined as the respective subsets of segment-feeding lines cross with the longlines.

9. The global switch matrix of claim 8 wherein the GSM further comprises:

(e) a seventh plurality, P of programmable interconnect points (PIP's) distributed at crosspoints of said longlines and said segment-feeding lines to implement a distributed multiplexing function for selectively coupling the GSM-sourced signals to respective but different ones of the segments;

(e.1) wherein respective subsets of said P PIP's are distributed to partially populate the longlines and segment-feeding lines crosspoints in an on-average uniform manner but in a locally non-uniform and pseudo-randomly varying manner.

10. The global switch matrix of claim 9 wherein:

(a.1) subsets of adjacent ones of the second plurality, L of longlines define a regular pattern of GSM output bands;

(e.2) respective ones of the P PIP's that are distributed along a given, first segment-feeding line are restricted to occupying a first subset of plural ones of said GSM output bands;

(e.3) respective other ones of the P PIP's that are distributed along a given, second segment-feeding line that is

adjacent to the first segment-feeding line are restricted to occupying a second subset of plural ones of said GSM output bands that is mutually exclusive of said first subset of plural ones of said GSM output bands so that collision of widths of the PIP's on said adjacent first and second segment-feeding lines is avoided by virtue of their respective PIP's occupying mutually exclusive ones of the GSM output bands.

11. The global switch matrix of claim **1** wherein:

(a.1) said second plurality, L of longlines are constituted by metal lines each having a width of about 1.6μ or more.

12. The global switch matrix of claim **11** wherein:

(a.2) said metal lines are further characterized by an inter-line spacing of about 0.5μ or more.

13. The global switch matrix of claim **1** wherein:

(a.1) said second plurality, L of longlines are defined by metal lines each having a width substantially greater than a standard line width prescribed for metal lines of said IC, where the greater width of the metal lines defining the longlines operate to minimize dominance in defining the RC delay of the longlines by a resistance value R of the longlines while the greater width of the metal lines defining the longlines do not operate to allow a capacitance value C of the longlines to dominate said definition of the RC delay of the longlines.

14. A global switch matrix (GSM) for use within a programmably configurable integrated circuit (IC), where the IC has a first plurality, S of segments distributed within a logic-functions providing region of the IC, where each segment has one or more logic blocks, said global switch matrix providing programmably-definable interconnection between logic blocks of different ones of said segments and said GSM comprising:

(a) a second plurality, L of longlines extending across the logic-functions providing region of the IC;

(b) a third plurality, G of segment-feeding lines crossing with the longlines and extending into the logic-functions providing region for coupling GSM-sourced signals from the GSM to corresponding ones of the segments,

(b.1) wherein respective subsets of said G segment-feeding lines that couple GSM-sourced signals to respective but different ones of the segments are intertwined as the respective subsets of segment-feeding lines cross with the longlines.

15. A monolithic, High-Density Complex Programmable Logic Device (HCPLD) for programmably implementing designs having parallel data words, said HCPLD having at least 64 I/O terminals for communicating with external circuitry, said HCPLD further comprising:

(a) a Global Switch Matrix (GSM);

(b) a plurality of logic-containing segments operatively coupled to the GSM; and

(b.1) wherein each segment has a plurality of macrocells which feed respective macrocell output signals directly to the GSM; and

(a.1) the GSM is sufficiently wide and each segment further has, as dedicated for inter-segment communications, at least as many longlines as there are macrocells in each of the plural segments, to thereby assure that every macrocell signal (MFB) of a first segment can be simultaneously transmitted through the GSM from the first segment to another of the plural segments.

16. A computer-implemented method for assigning respective ones of programmable interconnect points (PIP's) for partially-populating disposition at crosspoints of longlines and shortlines to thereby implement a distributed multiplexing function for selectively coupling longline-sourced signals to respective but different ones of the shortlines and wherein respective subsets of said PIP's are to be distributed to partially populate the longline and shortline crosspoints in an on-average uniform manner but in a locally non-uniform and pseudo-randomly varying manner, said method comprising:

(a) dividing the long lines into bands;

(b) initially distributing PIP locations in assigned pairs of bands for each of the shortlines;

(c) performing pair-wise, PIP-placement intersections tests for all unique permutations of comparable first and second shortlines (SL.a and SL.b);

(d) added and saving correlation results from the pair-wise testings of PIP placements of step (c);

(e) attempting a PIP-placement slide between bands;

(f) repeating the PIP-placement intersections tests for all unique permutations of the comparable first and second shortlines after the slide;

(g) adding the correlation results from the pair-wise testings of step (f) and comparing them against the saved results;

(h) identifying the results with lower correlation value, keeping the PIP placements associated with the identified lower correlation value, and defining as the saved results, the results associated with the identified lower correlation value; and

(i) repeating steps (e) through (h) until a PIP placements arrangement with a relatively minimized correlation value is found.

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